Abstract

A first device comprises a loop circuit to control a sample rate of a digital circuit element. A circuit comprises a digital loop circuit to control a sample rate of a digital circuit element to be a function of a frequency of a signal received by the circuit. A second device receives two or more sampled data streams having sample rates different from one another, converts the sample rate of one or more of the data streams to provide two or more data streams having sample rates compatible with one another, and combines the two data streams. Sample rate converter devices are used in a PLL and a clock recovery circuit.